Infrared Imaging Array Integrated in Three Dimensions Directly on Top of Silicon Circuits

Office of Naval Research Final Report

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SUMMARY

We have demonstrated the first three dimensional integration of a high quality compound semiconductor infrared imaging detector array directly on top of a foundry-produced silicon neuromorphic image processing circuit. There is great potential for this new technology in neuromorphic image processing applications. This new ability to construct complex locally connected neuromorphic focal-plane processors with direct massively parallel connections to high quality compound semiconductor imaging arrays will lead to new levels of sophistication in focal-plane processing.

During this research, thin film p-i-n and metal-semiconductor-metal (MSM) detectors were fabricated and tested. A four-by-four array of detectors was integrated onto a metallized silicon substrate and directly on top of an array of silicon circuits. The yield of each of these arrays was 100%, i.e., every detector was functional, and, in the integration onto silicon circuitry, every circuit underneath the detectors was also functional.

3-D LOCALLY CONNECTED INFRARED FOCAL-PLANE PROCESSING

We have developed a fabrication process for the three-dimensional integration of arrays of high quality thin-film compound semiconductor devices directly on top of foundry silicon signal-processing circuits. The array of compound semiconductor devices was composed of thin-film epitaxial GaAs p-i-n double heterostructure detectors. These detectors are separated from the growth substrate, aligned and deposited directly on top of the silicon signal-processing circuits using a modified epitaxial liftoff process developed previously at Georgia Tech. The vertical three-dimensional integration of the detectors on top of the silicon circuits is accomplished using a layer of insulating polyimide to planarize the silicon circuits. Metallized vias in this polyimide provide electrical connection between the silicon circuit and the detectors which lie on top of the polyimide. Throughout the development of this three dimensional integration process, low cost, high performance, standard, low impact fabrication techniques were used. The final layered structure has a top layer of detectors with high fill factor, connected to circuits below. The circuits are completely covered by the detectors and the detector fill factor is not related to the circuit complexity. The only impact on the circuits is the use of vias to connect the detector outputs to the circuit inputs. This vertical three-dimensional electrical interconnection scheme is completely parallel and therefore scales directly with the array size.

Focal Plane Processing Circuits

We designed and fabricated a number of different neuromorphic focal-plane processing circuits for this project, including a Mead-style retina, a current-mode retina, and a winner-take-all object-localization circuit similar to those developed by DeWeerth and Mead. We

fabricated several circuits with very different functionalities so that we would be able to test the behavior of the integrated detectors/circuits under the operating conditions presented by the various architectures. Each of these circuits contained vias (metal pads and overglass cuts) at every pixel so that it could be integrated with a detector array via epitaxial liftoff. Since the primary objective of this research was the demonstration of integration of a neuromorphic circuit with a GaAs IR detector array, we initially chose to integrate and test only one of these circuits. The selected circuit has been integrated and thoroughly tested as described below. We are currently in the process of integrating and testing additional circuits.

The first circuit that we chose to demonstrate the integration is a locally connected neuromorphic pulse-output processing array. This circuit is an array of the current-controlled subthreshold oscillators shown in Figure 1. This element converts the intensity of the light at the input of each detector to a frequency-encoded pulse train. This transformation is similar in form (but not in processing function) to the signal-type transformation that occurs in the mammalian retina which also converts receptor light intensity to ganglion-cell firing rate.

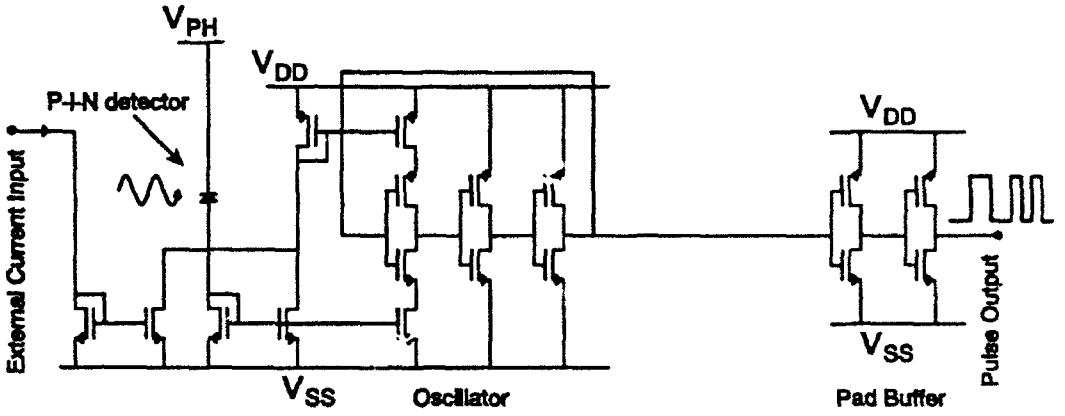

Figure 1. Subthreshold amplifier array element circuit.

An interesting application of this processing array can be generated when the outputs of the individual elements are added. When the output currents from all of the elements are added, a frequency domain signature of the image on the detectors is created. This serial signal can be transferred off chip on a single output pin. The resulting aggregated signal can then be processed by a neuromorphic temporal filter such as the Lyon/Mead electronic cochlea to extract the frequency information from the signal. The resulting signature would be translationally and rotationally invariant, and would be unique for a particular group of objects in any orientation against a fixed background.

This scenario has a startling similarity to the gross anatomy of biological image processing systems. The massively parallel locally interconnected focal plane circuitry processes the image in parallel to produce a compressed pulsed image representation that retains only key aspects of the image data. This is analogous, although much simplified, to the image compression performed by the primate retina using massively parallel local interconnect to produce the pulses that travel along the optic nerve. The use of temporal filtering to identify the various image signatures is analogous to the complexity of visual cortex used to process the retinal image signals. We do not propose that these simple circuits in any way duplicate neurobiological processing. However, the basic idea of using massively-parallel locally-connected focal-plane processing to produce a compressed image representation that

is uncompressed later at another locally connected neural processing site is the same as the principle observed in the biological architecture.

This demonstration architecture has the basic structure needed for useful applications in target identification and HDTV image processing. In target tracking applications, the focal plane processor could use massively parallel local connections to locate interesting features in the image plane and communicate only the local image data and coordinates to a tracking computer. In image compression applications, the locally connected focal plane circuitry could spatially and temporally filter the image and send the low spatial frequency image changes preferentially to the higher spatial frequency changes. This is essentially what the current standards for motion picture compression seek to do. We are currently investigating both of these applications and hope to perform continued research in these areas.

DETECTOR FABRICATION AND TEST

Thin Film GaAs Detectors

The study and optimization of thin film detectors for three dimensional integration with neural network imaging systems has progressed rapidly. Both MSM and p-i-n detectors have been investigated for this research. For the integration of the 4 X 4 array of detectors directly on top of silicon circuits, an array of double heterostructure AlGaAs/GaAs/AlGaAs p-i-n detectors was used due to the ease of fabricating a single common top contact for the entire array. This common contact is in contrast to dual top contacts which are necessary to integrate MSM detectors. In addition, the advantage of positioning the via for the vertical electrical interconnection directly underneath the detector can be accomplished using p-i-n detectors. Finally, the processes used to fabricate these GaAs-based detectors can be extended, with minor changes, to long-wavelength infrared multiple-quantum-well detectors for LWIR focal plane arrays.

We have investigated thin film p-i-n detectors at wavelengths of 850nm (GaAs/GaAlAs double heterostructure) and at 1300nm (InGaAsP/InP double heterostructures), which both display excellent performance. Measurements on these detectors show the lowest dark currents in thin film epitaxial devices to date, namely, 0.9 nA dark current and 0.56 A/W responsivity (unbiased) for the InGaAsP pin, and 22 pA (unbiased) and 29 pA (5 V) dark current for the GaAs pin detectors.

We have also demonstrated the first back contact MSM structure, and have shown that a rapid thermal anneal of the integrated detector structure produces a lower dark current and a higher responsivity than the unannealed detector. We have reported that the dark current improves by a factor of 2 at 5V bias with an anneal of 410 C for 20 seconds. The lowest MSM dark current reported to date in a thin film epitaxial lift off detector is 90 nA at 5V; the measured dark current of our thin film detectors after anneal is 1.2 nA, a substantial improvement! There is also a substantial improvement in the responsivity of the detector after annealing; for example, the response to 1.1 microwatt of incident power at a wavelength of 850 nm at 5V bias increased under annealing from 0.015 A/W to 0.1 A/W, again an outstanding increase in the performance.

THREE DIMENSIONAL VERTICAL INTEGRATION

Deposition and repair of array of detectors onto a silicon host substrate

In addition and prior to deposition of a four-by-four array of detectors onto an array of silicon circuits, a four by four array of thin film epitaxial lift off p-i-n GaAs based detectors has also been processed, aligned, and simultaneously deposited onto a oxide-coated silicon host substrate with metallized interconnect to individually address the pixels in the array. One of the devices was shorted to an address line, and we demonstrated that the faulty thin film device could be removed and replaced with a functional device. This was achieved through the alignment and deposition of a single device (or an array of devices), a capability which has been developed in the Georgia Tech transfer diaphragm process. This demonstrated repair capability is an important tool in a high pixel density manufacturing process.

Three dimensional integration using planarizing polyimide, vias and metallization

Integration was performed on the chips in an as-received condition from MOSIS. In the chip design, cuts in the overglass were made not only over the bonding pads, but also over the pads which would ultimately support the vias for three dimensional circuit integration. Polyimide was spun on in multiple coats and cured according to the schedule described in detail below. Square 20 micron x 20 micron vias in the polyimide were patterned using an aluminum hard mask and reactive ion etching (a mixed oxygen/fluorine chemistry) through the entire thickness of the polyimide. This etch exposed the circuit traces at the bottom of the via for subsequent interconnection. A layer of titanium which acted as a barrier metallization followed by a 0.35 micron-thick layer of gold was then deposited. This metal layer was patterned such that a contact was made between the now-exposed metal trace on the circuit, sloped up the sidewall of the via, and provided a contact pad for the chiplet. The chiplets were then deposited onto this gold pad using the Georgia Tech transfer-diaphragm technique. An additional layer of 3 micron-thick polyimide was then deposited to both insulate and "embed" the chiplets. To make contact to the upper chiplet surface, a via hole, slightly smaller than the chiplet perimeter, was etched through this polyimide. The upper contact to the chiplets was then made by blanket-depositing a trilayer film of gold-germanium / nickel / gold and patterning it to make a ring contact to each chiplet. This common blanket metallization completed the integration process by contacting the circuit through a common via.

More detail regarding the planarization process is discussed below. The polyimides used were successive dilutions of DuPont PI-2611 with N-methylpyrrolidone. A total of five coats were applied, with an intermediate bake step between coats. Before coating, the metal traces, which had to be planarized, were approximately 1.8 μm in height. After coating, the planarized step height was reduced to 0.4 microns, corresponding to a planarization of 76% (where 0% indicates no planarization and 100% indicates a perfectly smooth surface). The total thickness of polyimide which was applied was 14.5 microns. This allowed the fabrication of vias 20 microns on a side with very favorable aspect-ratio characteristics. Figure 2 shows a schematic of the structure which has been fabricated, while Figure 3 shows a photomicrograph of the actually-fabricated structure.

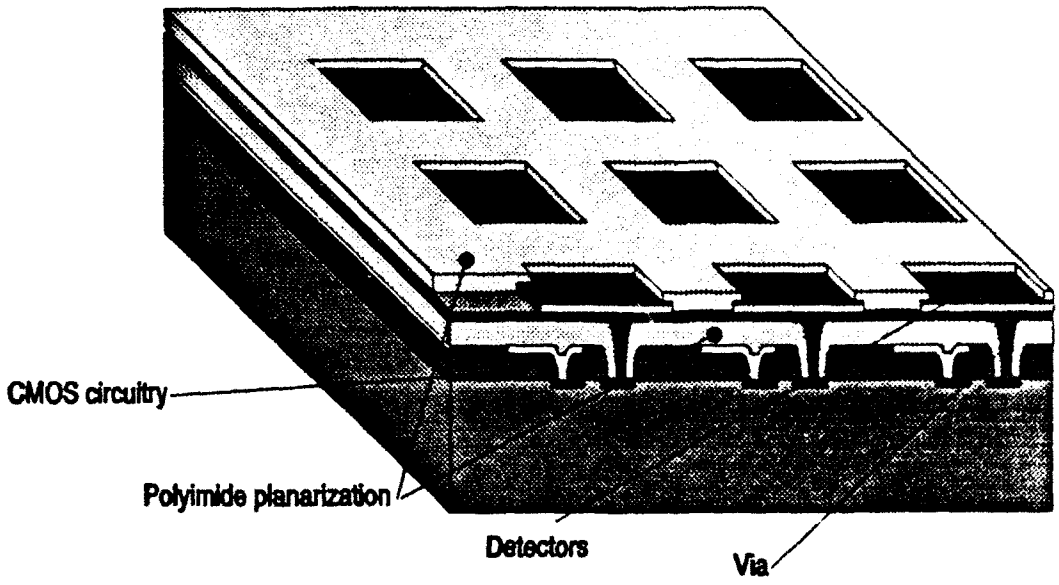

Figure 2. Schematic diagram of 4x4 array of vertically interconnected chiplets

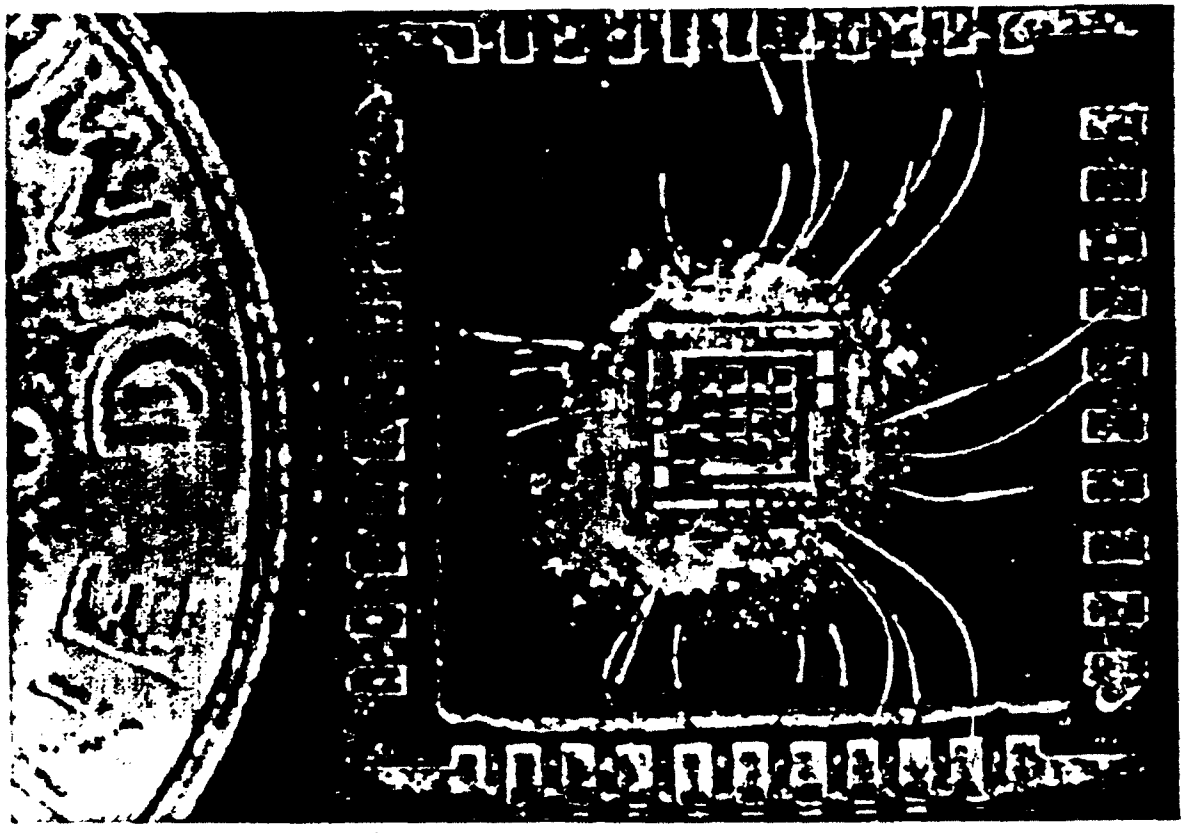

Figure 3. Photomicrograph of the fabricated circuit.

Thermal cycling of via chains and p-i-n detectors

In order to determine the mechanical stability of the proposed interconnect as a function of temperature, a set of test structures were fabricated and subjected to thermal cycling. These test structures consisted of via chains (i.e., a set of series-connected vias) in a two-level metal structure with a layer of DuPont PI-2611 polyimide as the interlayer dielectric. The bottom layer was 0.2 microns of titanium, and the top metal was 3 microns of aluminum. The wires ranged from 10-100 microns in length, and from 10-20 microns in width. The vias tested were of two sizes: ten microns on a side and twenty microns on a side. Via chains of lengths ranging from 22 to 24 vias were tested.

Photomicrographic examination of the via chains both before and after thermal cycling (immersion in liquid nitrogen (77 K) for 15 seconds (i.e., thermal shock), and subsequent rewarming up to room temperature) shows that there is no detrimental effect on the via mechanical structure. Electrical measurements of the vias also indicate the same electrical characteristics both before and after thermal shock. Thus, we are confident that the interconnect structure will be able to stand up to any required thermal cycling.

Thermal cycling measurements were also performed on a thin film p-i-n detector and a thin film p-n LED integrated on top of polyimide which was deposited on a silicon substrate; essentially the layer assembly of the three dimensionally integrated assembly. These assemblies were subject to the following thermal cycle: 15 sec at 77 K, 15 sec at 300 K, 15 sec at 400 K, 15 sec at 300 K. This cycle was repeated seven times. Measurements of the current-voltage (I-V) characteristic of each of the thin film devices was performed before the cycling and after the seven cycles were complete. There was no change in the p-i-n detector I-V characteristic due to thermal cycling, and there was no change in the p-n junction emitter I-V characteristic due to thermal cycling.

DEMONSTRATION OF 4X4 ARRAY OF GAAS IR DETECTORS ON SILICON NEUROMORPHIC IMAGE PROCESSING CIRCUIT

We have developed a generic technology for the monolithic integration of high quality thin-film epitaxial compound semiconductors with mass produced foundry silicon circuits. To demonstrate this technology GaAs heterostructure detectors were integrated with a locally-connected neuromorphic silicon image-processing circuit fabricated at the MOSIS foundry. As described above this circuit converted light input to the detectors into a frequency-encoded output. The finally product of the integration was an imager consisting of a four-by-four array of pixels as shown in the photograph in Figure 3.

Experimental Results

The first test that we performed showed that all sixteen detectors were indeed correctly connected to their respective circuit elements. We tested the success of the integration process by testing individually the response of each of the pixels to a light source. The test was performed using a binary light-off/light-on test of each pixel. The results were a resounding success, with each pixel showing near-zero firing rates with no light input and significant firing rate when exposed to the light source. Qualitatively, the pixels also seemed very reasonably well-matched, given that the respective firing rates of all of the pixels were very similar for each of the two states.

The next test was used to show that the pixels demonstrated a graded response to the light intensity. In this test, one pixel was chosen at random and exposed to a total of five different light intensities. The output response of the circuit element was measured for each

intensity. Figures 4 through 8 show the response of the pixel (displayed as oscilloscope traces) to monotonic increases in light intensity, with Figure 4 showing the response to no light and Figure 8 showing the response to the largest light intensity. Again, the response of the chip was excellent, with an obvious increase in firing rate demonstrated for each successive increase in light intensity.

IMPACT OF THIS WORK

Application to NAWS at China Lake LWIR Motion Detection and Target Tracking

The demonstrated technology has immediate application to ongoing work funded by the Naval Air Warfare Station at China Lake. Under the China Lake program Georgia Tech is developing motion detection and image jitter reduction focal plane circuits, and adapting the liftoff process for long wavelength IR detectors fabricated in GaAs using multiple quantum well material grown at China Lake. The vertical integration technology developed under ONR sponsorship will be applied to these detectors and circuits. Because of the separation of the circuit manufacturing, the detector manufacturing, and the integration processing, the ONR developed process is directly applicable without modification. The same GaAs AlGaAs liftoff selective etch can be used.

Published Results of this Research

M.C. Hargis and N.M. Jokerst, 'High Performance Thin Film GaAs/AlGaAs Metal-Semiconductor-Metal Photodetectors with Back Passivation', to be submitted to **IEEE Photonics Technology Letters**

K. Hirotsu and M.A. Brooke, 'Hardware Learning in Analog Integrated Neural Networks' to be submitted to **Neural Networks**

C. Camperi-Ginenset, Y. Wang, B. Buchanan, T.G. Morris, N.M. Jokerst, M.G. Allen, M.A. Brooke, and S.P. DeWeerth, 'Three-Dimensional Vertical Electrical Integration of Circuits and Opto-Electronic Devices' to be submitted to **IEEE Journal of Quantum Electronics**

B. Buchanan, T.G. Morris, C. Camperi-Ginenset, Y. Wang, M.A. Brooke, S.P. DeWeerth, N.M. Jokerst, and M.G. Allen, 'A Pulse-Coded Imager with Monolithically Integrated Silicon Circuits and GaAs Detectors' in progress

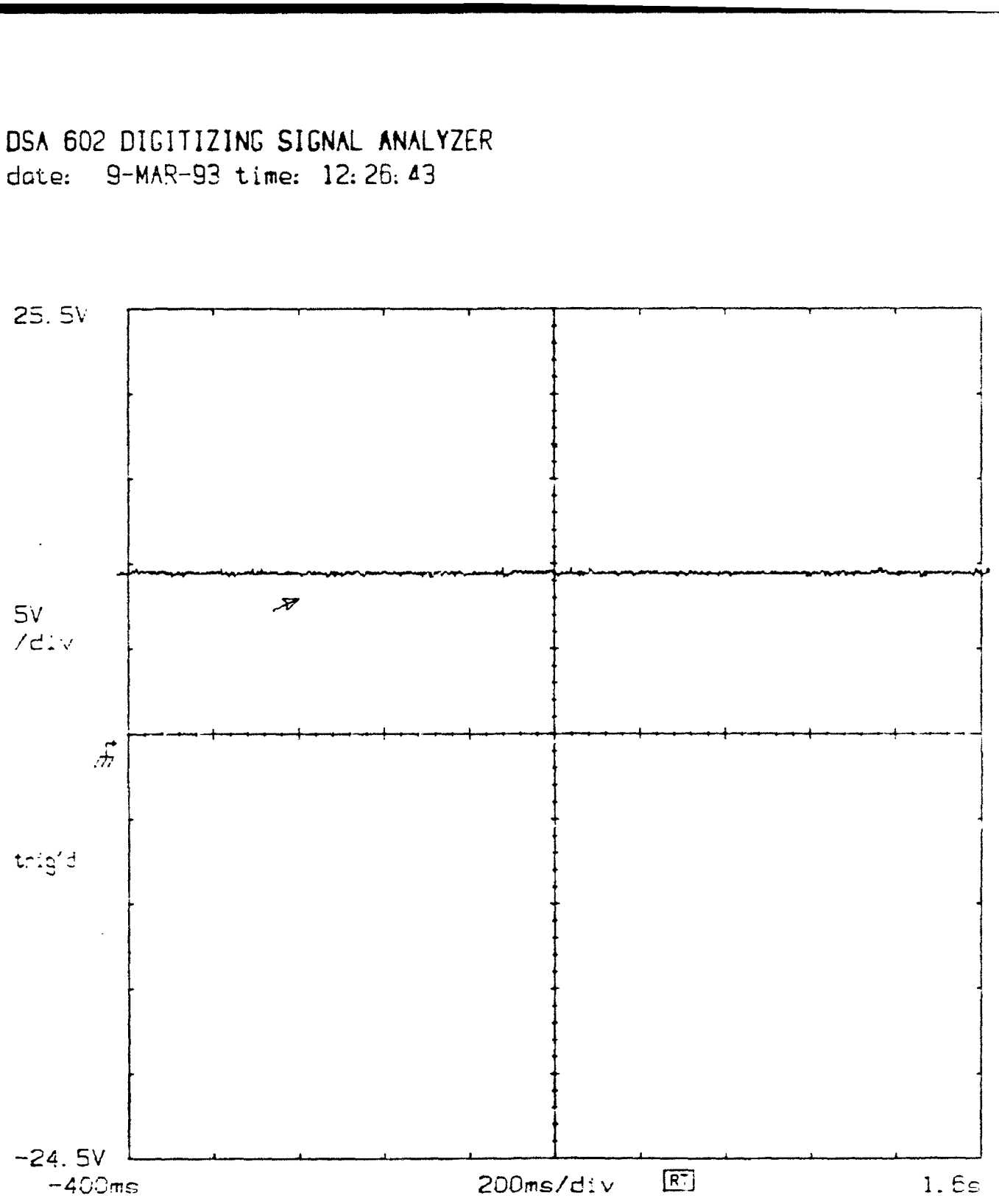

Figure 4. Output of one oscillator circuit pixel with no light incident on the detector.

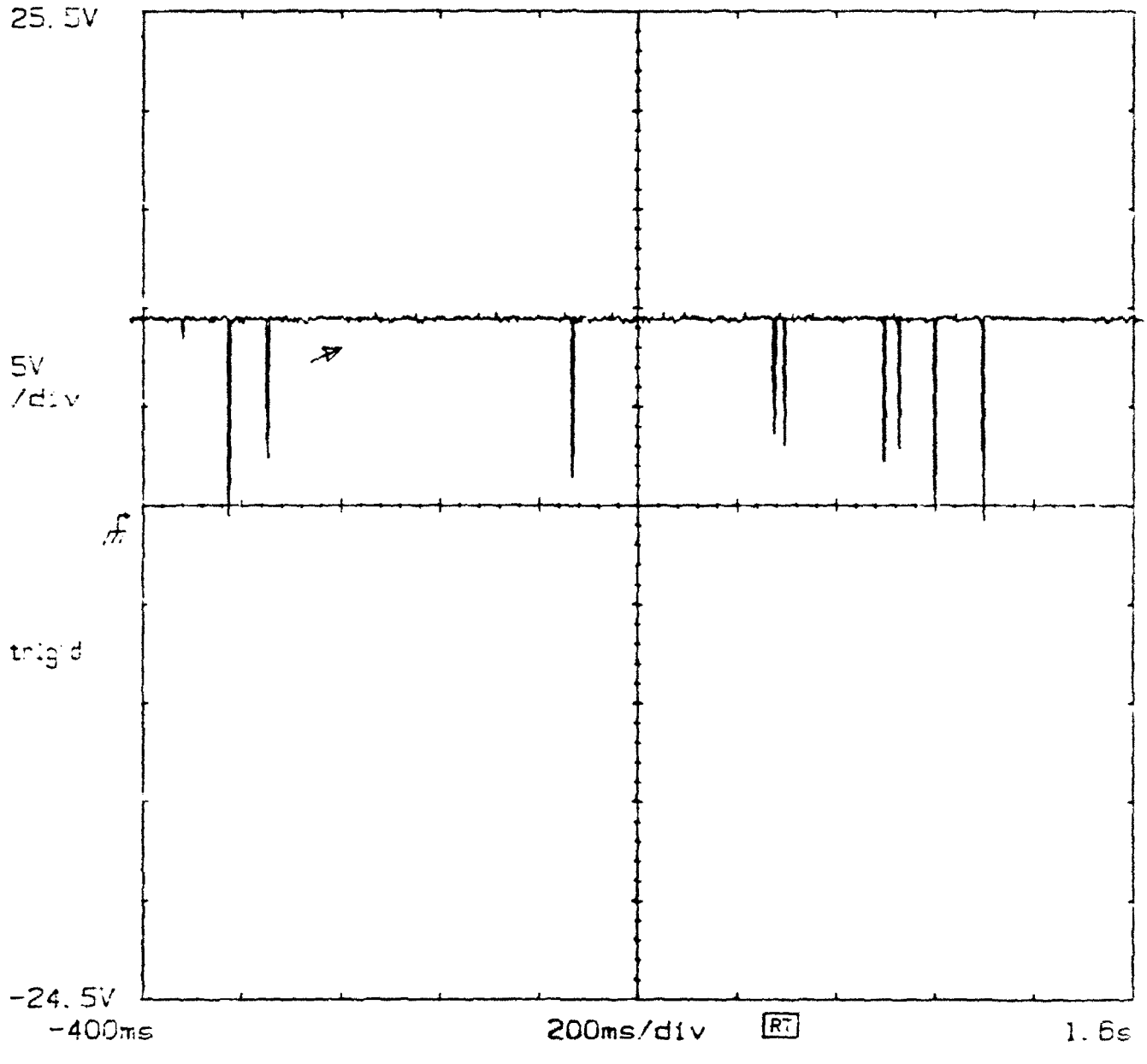

Figure 5. Output of one oscillator circuit pixel, with larger light intensity than the previous figure.

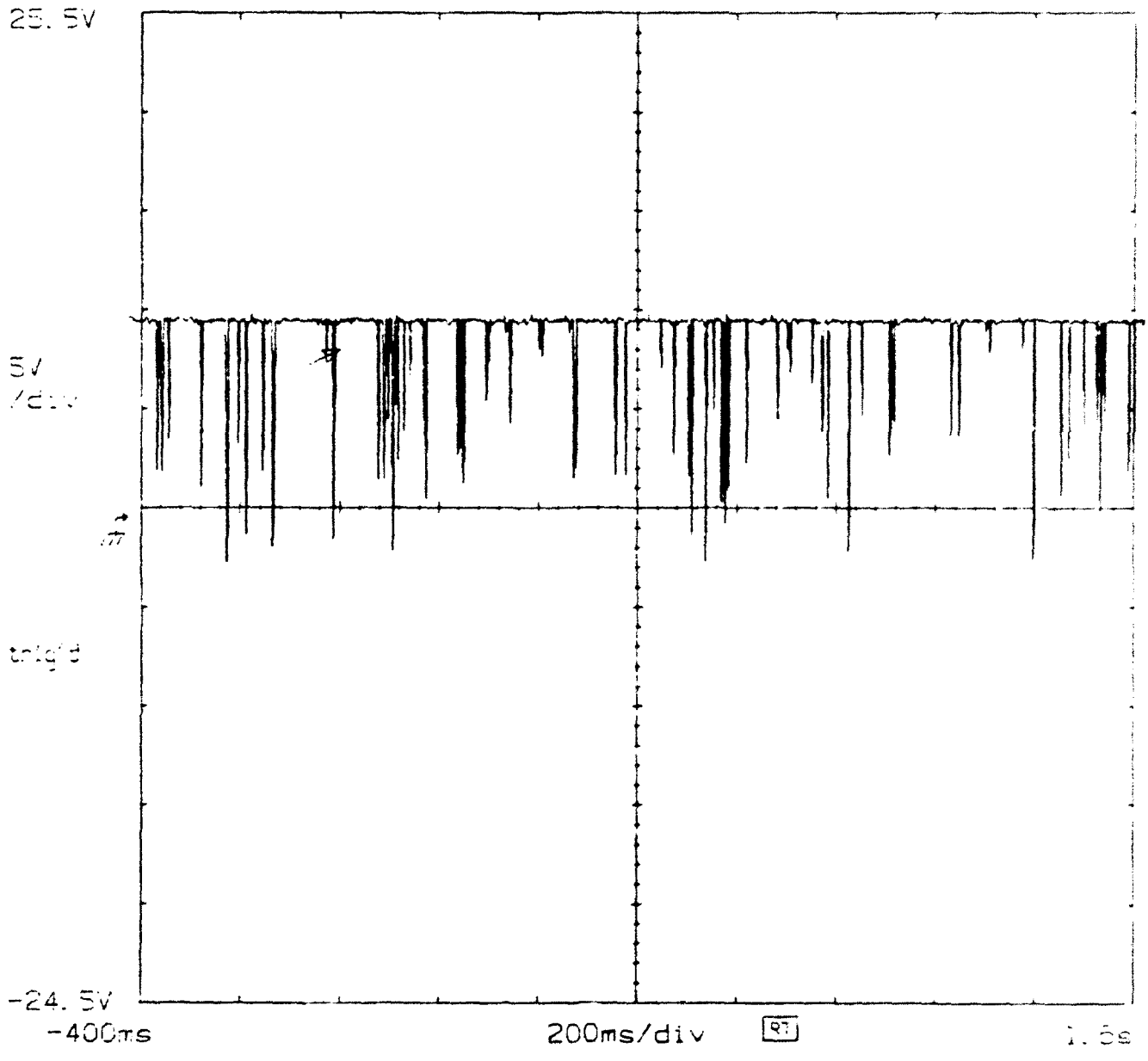

Figure 6. Output of one oscillator circuit pixel, with larger light intensity than the previous figure.

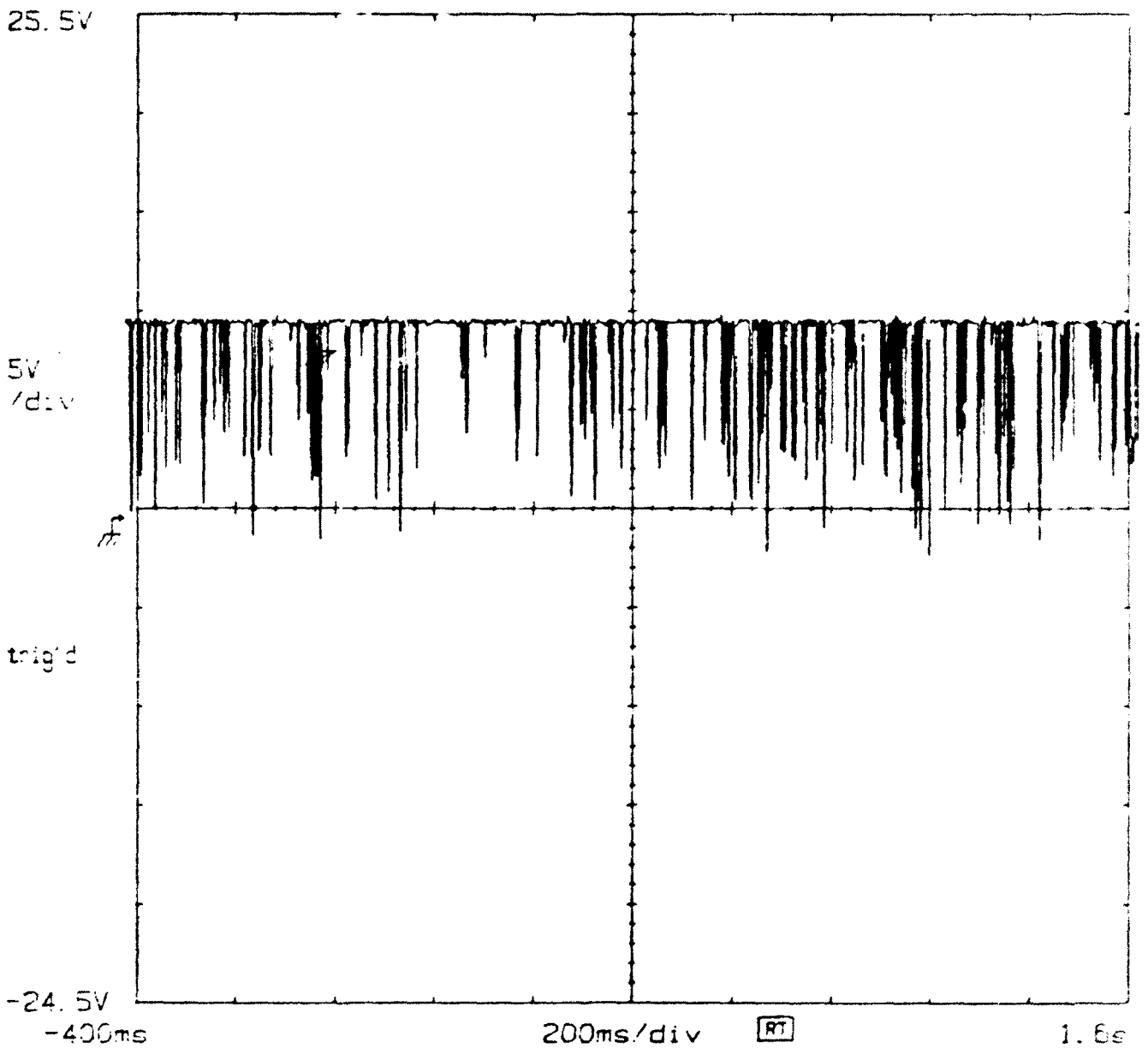

Figure 7. Output of one oscillator circuit pixel, with larger light intensity than the previous figure.

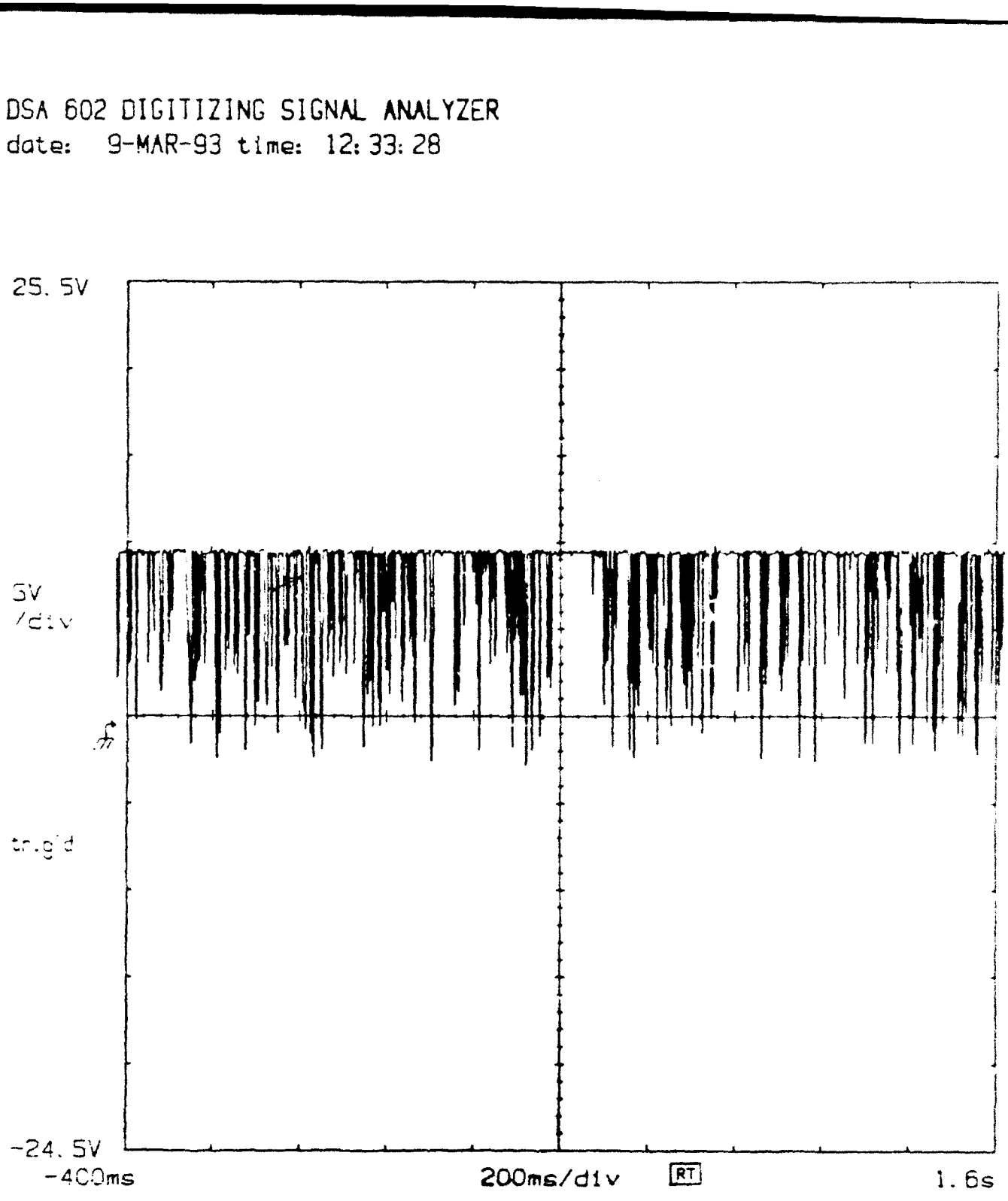

Figure 8. Output of one oscillator circuit pixel, with larger light intensity than the previous figure.

High Performance Thin Film GaAs/AlGaAs Metal-Semiconductor-Metal Photodetectors with Back Passivation

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Abstract

High performance thin film epitaxial lift off (ELO) photodetectors have great potential for integration with independently optimized integrated circuits and waveguides. The dark current and frequency response of GaAs/AlGaAs metal-semiconductor-metal (MSM) photodetectors which remain on the growth substrate are compared to thin film ELO detectors with and without back passivation in this paper. The passivated thin film detectors perform comparably to the on-wafer devices, while the unpassivated devices exhibit performance degradation. In addition to demonstrating the importance of back passivation, this paper presents the lowest ELO MSM detector dark current (5 nA at 5 V) publisheded to date.

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Introduction

The separation of single crystal, thin film compound semiconductor epitaxial devices from the growth substrate with subsequent bonding onto a dissimilar host substrate, called epitaxial lift off (ELO), is a promising technology for the low cost hybrid integration of epitaxial devices with host materials such as silicon, glass, and lithium niobate [1, 2, 3, 4]. One of the primary issues to be addressed in the ongoing evaluation of these thin film devices is that of performance in comparison to as-grown, on-wafer devices. Closely linked to performance evaluations are the optimization of device designs and fabrication processes specifically for thin film ELO devices. In this paper, we demonstrate that the back passivation, separation and bonding of thin film metal-semiconductor-metal (MSM) photodetectors results in a dark current and frequency response which are comparable to the on-wafer device, which is in sharp contrast to the unpassivated thin film MSM, which shows an increase in the dark current and a decrease in the frequency response. The dark currents reported herein also represent the lowest dark currents published to date (5 nA at 5V bias) for ELO thin film MSM detectors.

Fabrication

Three types of MSM detectors were fabricated to evaluate the impact of back passivation on the dark current and frequency response of thin film ELO devices. The first sample was not separated from the growth substrate (an on-wafer device), the second was separated from the growth substrate and bonded to the host without passivation, and the third device was back passivated, separated from the growth substrate, and bonded to the host substrate.

The epitaxial material used to fabricate all of the MSM detectors was grown on a GaAs substrate with a 100 nm AlAs sacrificial etch layer. The nominally undoped epilayers grown on top of the AlAs layer were a 30 nm thick $Al_{0.3}Ga_{0.7}As$ layer followed by a layer graded over 20 nm to GaAs, a 2 μm thick GaAs absorbing layer followed by a layer graded over 20 nm to $Al_{0.3}Ga_{0.7}As$, and a final layer of 30 nm of $Al_{0.3}Ga_{0.7}As$ to form a symmetric epitaxial device.

To form the MSM detectors, one of the samples was passivated with 20 nm of silicon nitride. All of the epitaxial material was then mesa etched into 200 μm diameter mesas using standard photolithography and wet etching. The mesa definition etched through the epitaxial material to, but not through, the AlAs sacrificial etch layer used to separate the thin film devices from the growth substrate. The two ELO samples were subsequently coated with an Apiezon W handling layer and separated from the growth substrate through selective etching of the AlAs sacrificial etch layer [1].

A key to the back side passivation of the MSM detectors is the ability to process both sides of the thin film device. Using the transfer diaphragm technique, a modified ELO process, it is possible to process both sides of the thin film device while it is under either growth or host substrate support [5]. After separation, the two thin film samples embedded in the Apiezon W were bonded to a transparent polyimide transfer diaphragm and the Apiezon W handling layer was removed with trichloroethane. The diaphragm was then inverted and the thin film devices were deposited onto nitride-coated silicon host substrates. Note that the passivated side of the MSM passivated detector is facing the silicon host substrate (i.e., the MSM device has been inverted).

To define the interdigitated finger contacts on all three MSM samples, the devices were first planarized with photosensitive polyimide. Windows in the polyimide were opened, and interdigitated Schottky electrodes with finger widths of 1.5 μm and spacing of 3.5 μm were defined in Ti/Au metallization using contact photolithography and metal lift off. A schematic cross section of the passivated thin film MSM detector is shown in Figure 1. The front surface of each of the detectors was compensated with the AlGaAs epitaxial window layer.

Results

The dark current as a function of voltage was measured for all three of the MSM detectors, and is shown in Figure 2. The passivated thin film detector has a dark current of 5 nA at a 5 V bias, which is comparable to the on-wafer dark current of 2 nA at a 5 V bias. In sharp contrast, the unpassivated thin film device exhibits a dark current of 66 nA at a 5 V bias. This unpassivated thin film device also shows evidence of low frequency gain in the current-voltage (I-V) characteristic, as indicated by the increase in the slope of the I-V characteristic at 4 V. This may be due to an increase in the number of surface states at the unpassivated, separated surface. The demonstration of trap-induced low frequency gain in GaAs MSM detectors [6, 7] supports this hypothesis.

The photoresponse of all of the MSM detectors was measured with 200 μW of input power at a wavelength of 850 nm, as shown in Figure 3. The responsivity of the back passivated thin film device (0.38 A/W) compares well to the on-wafer MSM (0.47 A/W), but the unpassivated thin film device shows a degradation in the responsivity (0.14 A/W). In addition, both of the thin film MSM detector photoresponse curves display a rounding of the knee of the curve. This rounding may be due to increased carrier recombination at the surfaces, which causes charge storage in the photodetectors. To saturate an MSM detector photoresponse, equilibrium between the carrier recombination rate and the carrier conduction rate must be achieved [8]. Thus a higher carrier recombination rate will result in a higher saturation voltage with a corresponding larger electric field, to separate the photogenerated

electron-hole pairs and sweep them to the contacts before they recombine at a surface, which results in a lower responsivity at low bias voltages. This effect is evident in the thin film device photoresponse curves, in which the passivated thin film MSM photoresponse saturates at 1.5 V, and the unpassivated saturates at 4 V. Rounding of the photoresponse curves is less pronounced in the passivated thin film detector than in the unpassivated case, however, the evident rounding in both cases suggests that the recombination velocity for the nitride/AlGaAs (passivated) interface is higher than that for the AlAs/AlGaAs (on-wafer) interface. Other passivating layers may produce a lower recombination velocity and reduce the photoresponse saturation voltage and the rounding of the photoresponse curve.

The frequency response of the three MSM detectors was measured with a lightwave component analyzer at a wavelength of 850 nm which was modulated from 130 MHz to 3 GHz. The detector was sighted within a coplanar transmission line with an impedance of 50 Ω. Figure 4 shows the measured frequency response of the three detectors. The 3 dB frequency is 1.9 GHz for the passivated thin film device, 2.0 GHz for the on-wafer detector, and 0.85 GHz for the unpassivated thin film MSM. The reflection at slightly above 2 GHz which is evident for the two thin film MSM detectors is probably due to an impedance mismatch at the MSM/host substrate interface. The reflection for the passivated thin film detector occurs at a slightly higher frequency than the unpassivated device, which is consistent with the presence of the dielectric passivation layer at the back surface of the detector.

Conclusions

The back passivation of thin film MSM detectors which have been separated from the growth substrate and bonded to a host substrate significantly improves the performance of the thin film device when compared to unpassivated thin film devices. The reported dark current is the lowest published to date for an ELO thin film MSM detector. The passivated device performance approaches that of the on-wafer devices, however, the measured results indicate

that better passivation of the back surface to further reduce the surface recombination velocity may result in further performance improvement.

Acknowledgements

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Figure Captions

Figure 1. Schematic cross section of a back passivated ELO MSM detector. The epitaxial thin film consists of a symmetric graded double heterostructure.

Figure 2. Dark current-voltage characteristics of the back passivated thin film ELO MSM (ELO-BP), the unpassivated thin film ELO MSM (ELO-NP) and the on-wafer MSM.

Figure 3. Photoresponse of the back passivated thin film ELO MSM (ELO-BP), the unpassivated thin film ELO MSM (ELO-NP) and the on-wafer MSM.

Figure 4. Frequency response of the back passivated thin film ELO MSM (ELO-BP), the unpassivated thin film ELO MSM (ELO-NP) and the on-wafer MSM.

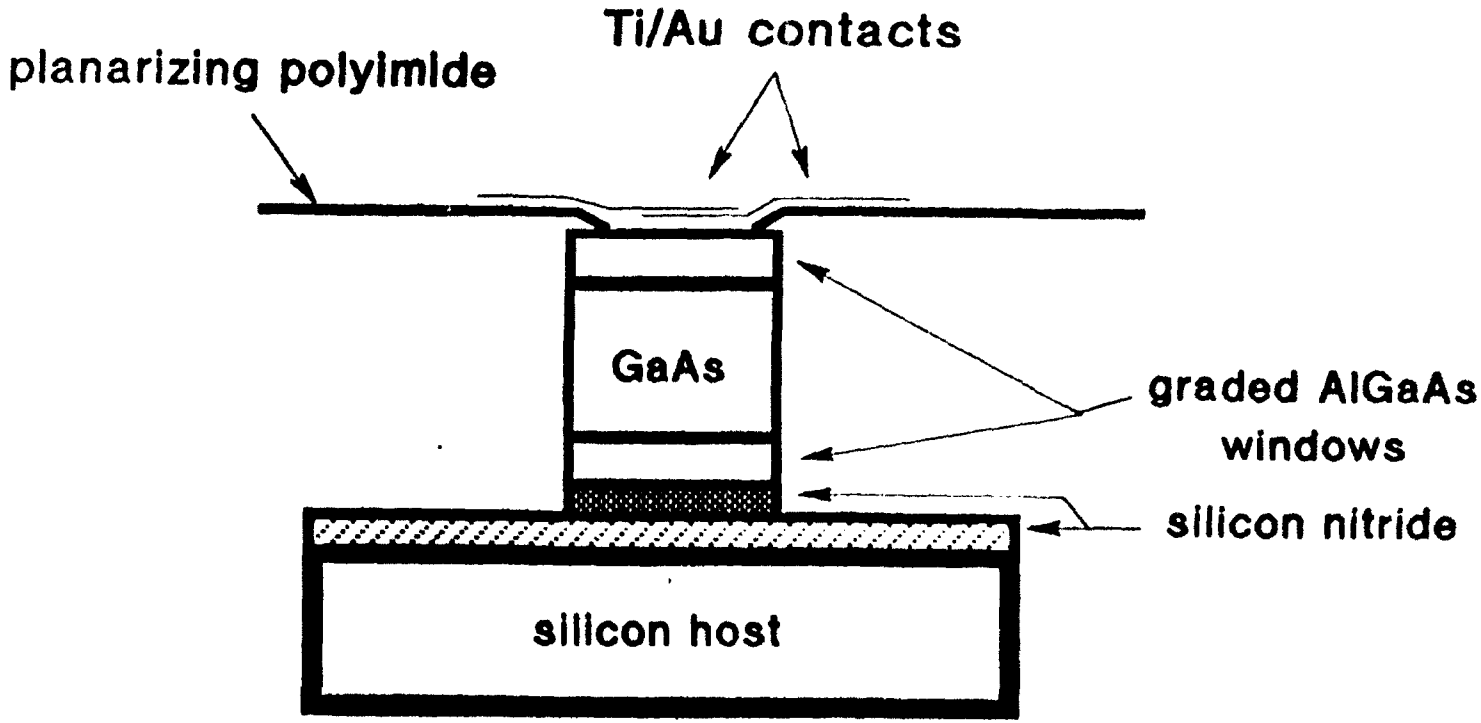
planarizing polyimide
Ti/Au contacts
GaAs
graded AlGaAs
windows
silicon nitride
silicon host

Fig 1

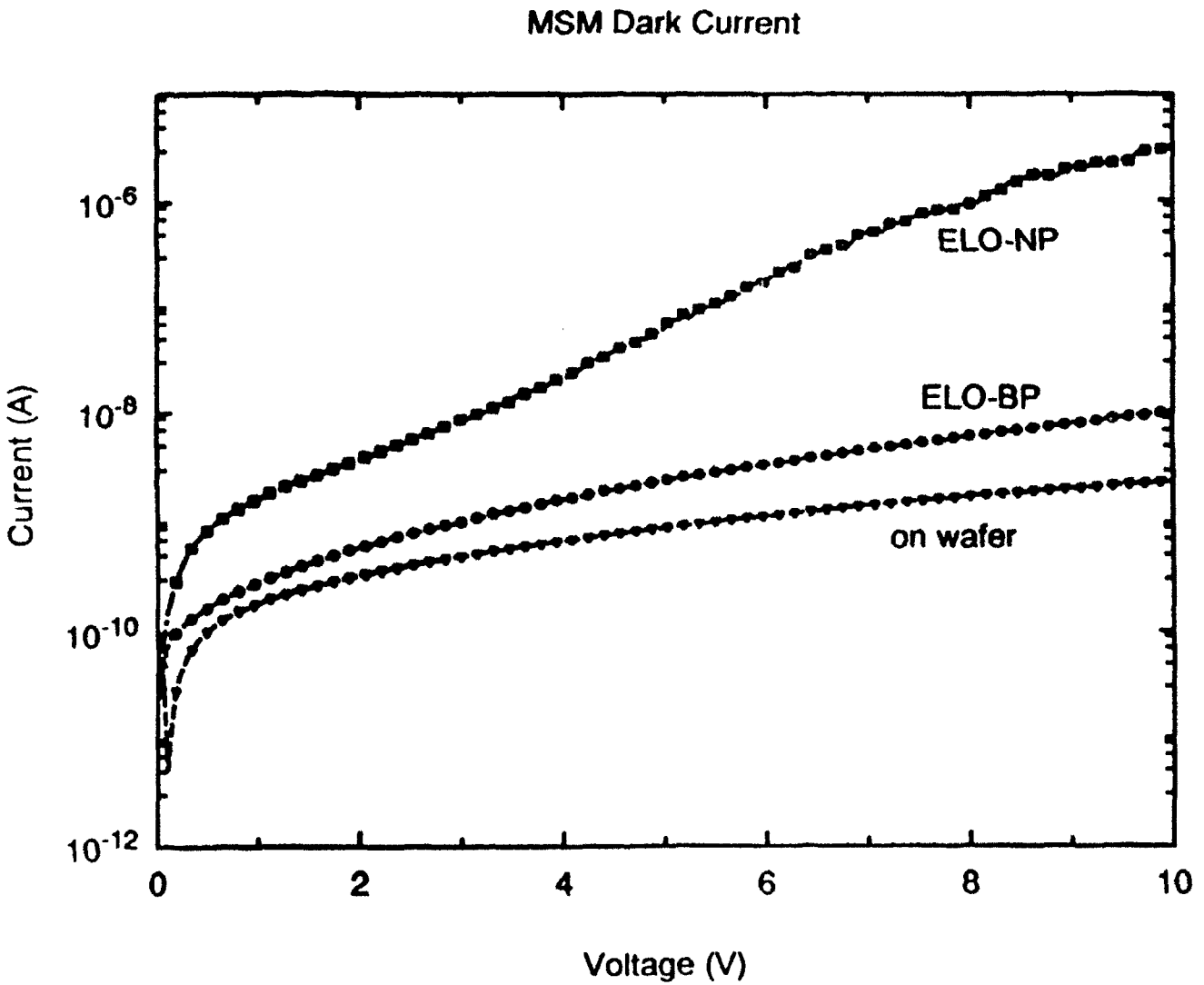
MSM Dark Current
Current (A)
10^{-6}
10^{-8}
10^{-10}
10^{-12}
ELO-NP
ELO-BP
on wafer
0
2
4
6
8
10
Voltage (V)

Fig 2

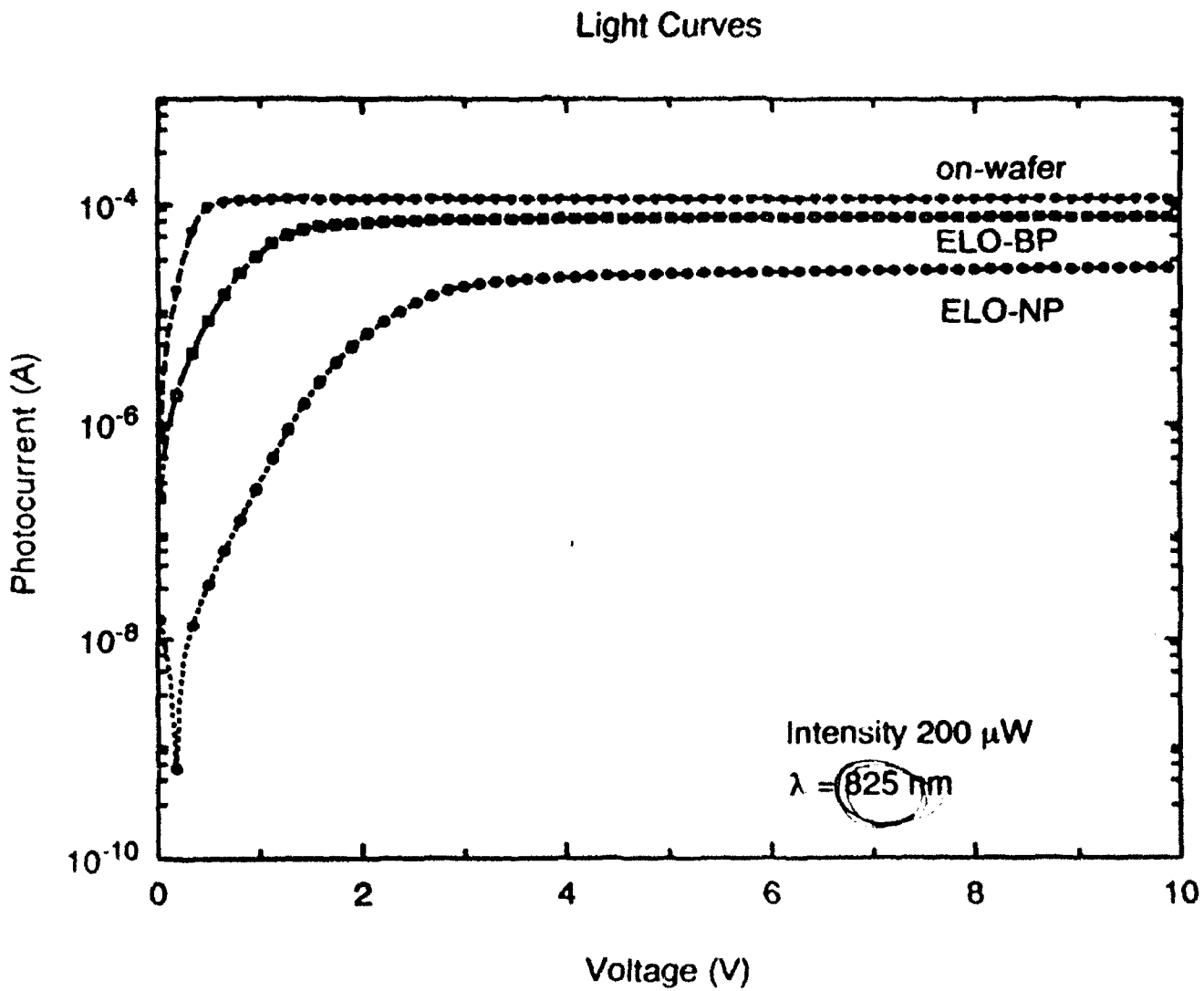
Light Curves
on-wafer
ELO-BP
ELO-NP
Intensity 200 μW
λ = 825 nm
Photocurrent (A)
10-4
10-6
10-8
10-10
0
2
4
6
8
10
Voltage (V)

Fig 3

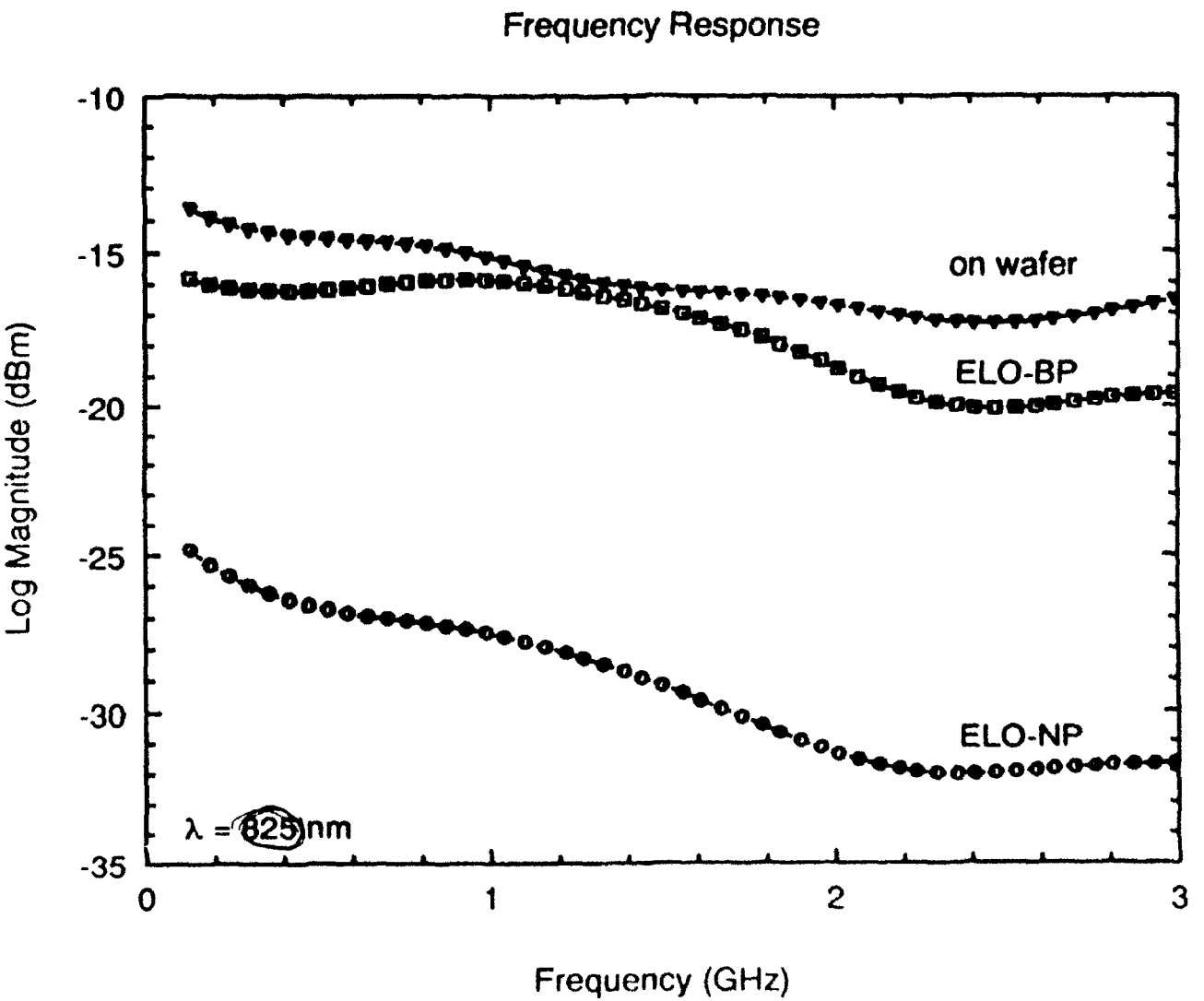
Frequency Response
-10
-15
-20
-25
-30
-35
Log Magnitude (dBm)
on wafer
ELO-BP
ELO-NP
λ = 825 nm
0
1
2
3
Frequency (GHz)

Fig 4